

IN THE CLAIMS:

The status of the claims is as follows:

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1. (Original) A method of fetching processor instructions, the method comprising:  
receiving a request for an instruction;  
searching a cache system at a first level for the instruction; and  
searching the cache system at a second level for the instruction in parallel with the first level based on a prediction of whether the instruction will be found at the first level.
  2. (Currently Amended) The method of claim 1 further including:  
determining a parameter value corresponding to a first level search history for the instruction;  
comparing the parameter value to a predetermined threshold; and  
initializing the search of the cache system at the second level if [when] the parameter value exceeds the predetermined threshold.
  3. (Original) The method of claim 2 further including determining a cache miss value corresponding to the first level search history.
  4. (Original) The method of claim 3 further including tracking a number of cache misses for a predetermined number of cache searches corresponding to the instruction.

5. (Currently Amended) The method of claim 4 further including initializing the search of the cache system at the second level if [when] the number cache misses for the predetermined number of cache searches is greater than zero.

6. (Original) The method of claim 2 further including storing the parameter value to a computer readable storage medium.

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7. (Original) The method of claim 6 further including storing the parameter value in the cache system.

8. (Original) The method of claim 2 further including retrieving the parameter value from a computer readable storage medium.

9. (Original) The method of claim 8 further including retrieving the parameter value from the cache system.

10. (Original) The method of claim 1 further including receiving a front end re-start instruction.

11. (Original) The method of claim 1 further including searching the cache system at a trace cache level for the instruction, the trace cache level being the first level of the cache system.

12. (Original) The method of claim 1 further including searching an instruction cache for the instruction, the instruction cache being the second level of the cache system.

13. (Original) The method of claim 1 further including searching the cache system at a main memory level for the instruction, the main memory level being the second level of the cache system.

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14. (Currently Amended) A method of searching a cache system at a second level, the method comprising:

determining a parameter value corresponding to a first level search history for an instruction;

comparing the parameter value to a predetermined threshold; and

initializing a search of the cache system at the second level if [when] the parameter value exceeds the predetermined threshold, wherein the search for the instruction at the second level is to be conducted in parallel with a search of the cache system for the instruction at the first level.

15. (Original) The method of claim 14 further including determining a cache miss value corresponding to the first level search history.

16. (Original) The method of claim 15 further including tracking a number of cache misses for a predetermined number of cache searches corresponding to the instruction.

17. (Original) The method of claim 15 further including initializing the search of the cache system at the second level when the number cache misses for the predetermined number of cache searches is greater than zero.

18. (Original) The method of claim 15 further including storing the parameter value to a computer readable storage medium.

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19. (Original) The method of claim 15 further including retrieving the parameter value from a computer readable storage medium.

Claims 20-23 (Canceled).

24. (Original) A computer readable storage medium storing a set of instructions capable of being executed by a processor to:

receive a request for an instruction;

search a cache system at a first level for the instruction; and

search the cache system at a second level for the instruction in parallel with the first level based on a prediction of whether the instruction will be found at the first level.

25. (Currently Amended) The storage medium of claim 24 wherein the set of instructions are further capable of being executed by the processor to:

determine a parameter value corresponding to a first level search history for the instruction;

compare the parameter value to a predetermined threshold; and

initiate the search of the cache system at the second level if [when] the parameter value exceeds the predetermined threshold.

26. (Currently Amended) A processor instruction management system comprising:

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an execution core to execute the decoded instruction, the instruction supply engine to search [searching] the cache system at a first level for the instruction and to search [searching] the cache system at a second level for the instruction in parallel with the first level based on a prediction of whether the instruction will be found at the first level.

27. (Currently Amended) The instruction management system of claim 26 wherein the instruction supply engine further includes:

a shift register to receive a first level search history signal for the instruction, the signal defining a number of cache misses for a predetermined number of cache searches corresponding to the instruction; and

an OR gate coupled to the shift register, the OR gate generating a miss prediction signal if [when] the number of cache misses for the predetermined number of cache searches is greater than zero.

28. (Currently Amended) The instruction management system of claim 27 wherein the shift register has three data outputs, the predetermined number of cache searches to be [being] three.

*A2 level*  
29. (New) The method of claim 1, further including fetching the instruction from the second level if the instruction is found at the second level and the instruction is not found at the first level, decoding the instruction and providing the decoded instruction to an execution core.

30. (New) The storage medium of claim 24, wherein the set of instructions are further capable of being executed to:

fetch the instruction from the second level if the instruction is found at the second level and the instruction is not found at the first level;

decode the instruction; and

provide the decoded instruction to an execution core.

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